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DOCKET NO.: S1022.80927US01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Jean-Michel RAVON	
Serial No.:	10/782,188	Patent No. 6,885,174
Filed:	February 19, 2004	Issued: April 26, 2005
For:	SYSTEM FOR PROVIDING A REGULATED VOLTAGE TO SUPPLY A LOAD	
Examiner:	Adolf D. Berhane	
Art Unit:	2838	Confirmation No.: 4106

ATTN: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

Transmitted herewith for filing is/are the following document(s):

[X] Request for Certificate of Correction
[X] Copies of: Page 8 of Apl. as Filed and Col. 6 of U.S. 6,885,174
[X] PTO Form SB/44
[X] Return Post Card

If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned collect at (617) 646-8000, Boston, Massachusetts.

No check is enclosed. If it is determined that a fee is necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to ATTN: Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on May 2, 2005.

Gail Driscoll

Attorney Docket No.: S1022.80927US01
XNDDX

Respectfully submitted,

Jean-Michel Ravon, Applicant

By: [signature]

James H. Morris
Reg. No.: 34,681
WOLF, GREENFIELD & SACKS, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210
Tel. (617) 646-8000

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REQUEST FOR CERTIFICATE OF CORRECTION

Sir/Madam:

Patentee respectfully requests the correction of an error found in the above-captioned patent. Specifically, there is a typographical error in column 6 of issued U.S. Patent No. 6,885,174.

As originally filed the paragraph on page 8, line 31 read as shown below:

> It should be noted that, since circuits 10 and 11 are independent from each other and operate **asynchronously**, other adapted current sources may be used. In particular, source 11 may be formed of a linear current regulator. (Emphasis added)

However, the corresponding text found in column 6, on lines 25-28 reads as shown below:

> It should be noted that, since circuits 10 and 11 are independent from each other and operate **a synchronously**, other adapted current sources may be used. In particular, source 11 may be formed of a linear current regulator. (Emphasis added)

No amendment was made by either the Examiner or Patentee to cause the word "asynchronously" to be changed to "a synchronously" in column 6, line 26 of issued U.S. Patent No. 6,885,174.

In support of this request Patentee encloses a highlighted copy of page 8 of the application as filed and column 6 of issued U.S. Patent No. 6,885,174. Also enclosed is PTO form SB/44.

The correction requested does not involve change in the patent that constitutes new matter or would require reexamination. Therefore, it is respectfully requested that the correction be made and that a Certificate of Correction be issued.

Patentee respectfully submits that, since the error for which a Certificate of Correction is sought was the result of Patent Office mistake, no fee is due. However, if the Examiner deems a fee necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825.

Should any questions arise concerning the foregoing, please contact the undersigned at the telephone number listed below.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to ATTN: Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on May 2, 2005.

Gail Driscoll

Attorney Docket No.: S1022.80927US01
XNDD

Respectfully submitted,

Jean-Michel Ravon, Applicant

By: James H. Morris

James H. Morris
Reg. No.: 34,681
WOLF, GREENFIELD & SACKS, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210
Tel. (617) 646-8000

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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,885,174

DATED : April 26, 2005

INVENTOR(S) : Jean-Michel Ravon

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 6, line 26 should read:
--independent from each other and operate asynchronously,--

MAILING ADDRESS OF SENDER

PATENT NO. 6,885,174

James H. Morris
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210

of transistors M1 and M2, and the recharge time would considerably decrease if the series resistance was too high.

Amplifiers of circuit 13 and capacitors 14 having fast response times will preferably be chosen to precisely control the output voltage. As a specific example, for a voltage Vout of 2.1 volts and an accuracy of ±5 % (±1 % for the accuracy of the reference voltage and ±4 % for the hysteresis), a 250 nanosecond delay in the response of comparator 14 and of circuit 13 increases voltage Vout by 68 mV with C' = 40 μF and I = 11 A (low charge). At high charge, voltage Vout decreases by 68 mV. It will thus be provided to reduce the hysteresis of comparator 14 by an equivalent value to keep a voltage Vout within imposed tolerance limits.

An advantage of the present invention is that output voltage Vout is practically independent from abrupt variations of the current due to microprocessor 2. Indeed, voltage Vout is comprised between two fixed hysteresis thresholds.

Another advantage of the present invention is that it is not necessary to have, within the converter, a fast response loop that would make the circuit more complex.

Another advantage of the present invention is that it decreases the size of output capacitor C' (as a specific example, a ceramic capacitor of 40 μF is sufficient), or even to use the decoupling capacitors generally implanted with the microprocessor (for example, 40 capacitors of 1 μF). Preferably, circuit 11 and device 10 are implemented in the form of separated units and device 10 is implanted as close as possible to microprocessor 2 to use these decoupling capacitors.

Another advantage of the present invention is that it increases the reliability of the microprocessor power supply by suppressing the use of chemical capacitors which have a low lifetime. Further, voltage Vout, which is not subjected to the drifts of chemical capacitors, is then determined precisely.

Still another advantage of the present invention is that it only places, in the vicinity of the microprocessor, regulation device 10 which is of limited size, and moves current source unit 11, which is more bulky, further away from microprocessor 2 on the implantation board.

It should be noted that, since circuits 10 and 11 are independent from each other and operate asynchronously, other adapted current sources may be used. In particular, source 11 may be formed of a linear current regulator.

transistor M3 and the midpoint of the series association of transistors M3 and M4, and controls circuit 17. A chemical filtering capacitor C is placed between terminal 16 and the ground.

A feature of this embodiment is that transistor M3 is, like previously-described transistor M2, controlled to operate in the linear portion of its current-voltage characteristic, to minimize the power dissipation, while circuit 11 generates, permanently, a current I corresponding to the maximum current (for example, on the order of 10 A) that load 2 is likely to surge. Current I in inductance L is controlled by circuit 17 by means of current detector 18, for example, a current transformer, a detection transistor, or any other adapted device. Inductance L is sized so that the minimum value of the current flowing therethrough is higher than or equal to the minimum value of the current surged by the load. Thus, the current ripple in inductance L does not influence the output voltage. The maximum current likely to be surged by load 2 is increased by on the order of 10%.

As long as voltage Vout across capacitor C' (FIG. 2) has not reached a minimum value, inductance L and transistor M2 and M4 are used to circulate current I freely. When the desired voltage Vout is reached, transistor M2 is blocked and transistor M1 is turned on after a slight idle time during which current I of inductance L flows through intrinsic diode D of transistor M1. Then, current I flows through turned-on transistor M1, and recharges capacitor C' to a maximum value. The minimum and maximum values correspond to the variation range of the hysteresis of comparator 14. Current I remains practically constant during the charge of capacitor C' and is equal to the chosen maximum current. The current ripple in inductance L increases during the recharge of capacitor C' since inductance L demagnetizes under the output voltage during a time which can reach the entire period of the cut-off frequency of circuit 17.

It should be noted that transistor M4 may possibly be replaced with a Schottky diode. However, using a MOS transistor has the advantage of leading to a better efficiency.

The value of capacitor C' is chosen according to the desired charge/discharge frequency and to the desired output current. At low charge, the capacitor is practically recharged by the entirety of the current available in inductance L. Thus, capacitor C' charges very fast while its discharge is very low. The constraints of voltage stability and rapidity of response to the variations of the current surged by the load are thus respected.

According to the present invention, a ceramic capacitor C' is chosen to exhibit a very low equivalent series resistance (ESR) (in practice lower than approximately 5 mΩ). Indeed, at low charge, capacitor C' charges with the maximum current at the switching of transistors M1 and M2, and the recharge time would considerably decrease if the series resistance was too high.

Amplifiers of circuit 13 and capacitors 14 having fast response times will preferably be chosen to precisely control the output voltage. As a specific example, for a voltage Vout of 2.1 volts and an accuracy of ±5% (±1% for the accuracy of the reference voltage and ±4% for the hysteresis), a 250 nanosecond delay in the response of comparator 14 and of circuit 13 increases voltage Vout by 68 mV with C'=40 μF and I=11 A (low charge). At high charge, voltage Vout decreases by 68 mV. It will thus be provided to reduce the hysteresis of comparator 14 by an equivalent value to keep a voltage Vout within imposed tolerance limits.

An advantage of the present invention is that output voltage Vout is practically independent from abrupt variations of the current due to microprocessor 2. Indeed, voltage Vout is comprised between two fixed hysteresis thresholds.

Another advantage of the present invention is that it is not necessary to have, within the converter, a fast response loop that would make the circuit more complex.

Another advantage of the present invention is that it decreases the size of output capacitor C' (as a specific example, a ceramic capacitor of 40 μF is sufficient), or even to use the decoupling capacitors generally implanted with the microprocessor (for example, 40 capacitors of 1 μF). Preferably, circuit 11 and device 10 are implemented in the form of separated units and device 10 is implanted as close as possible to microprocessor 2 to use these decoupling capacitors.

Another advantage of the present invention is that it increases the reliability of the microprocessor power supply by suppressing the use of chemical capacitors which have a low lifetime. Further, voltage Vout, which is not subjected to the drifts of chemical capacitors, is then determined precisely.

Still another advantage of the present invention is that it only places, in the vicinity of the microprocessor, regulation device 10 which is of limited size, and moves current source unit 11, which is more bulky, further away from microprocessor 2 on the implantation board.

It should be noted that, since circuits 10 and 11 are independent from each other and operate a synchronously, other adapted current sources may be used. In particular, source 11 may be formed of a linear current regulator.

FIG. 4 illustrates an alternative implementation of the present invention in which transistor M1 and its intrinsic diode D are replaced with a Schottky diode D1. Such an alternative avoids using a level shifting and timing circuit 13. Indeed, since the direction of the current is imposed by diode D1, it is no longer required to delay the turning-on to set the current direction with intrinsic diode D of the MOS transistor. Further, diode D1 does not require any control signal. However, the use of a transistor rather than a Schottky diode has the advantage of providing a better efficiency.

In FIG. 4, an embodiment of hysteresis comparator 14, an output of which directly controls transistor M2 for which a level shifter is no longer necessary, has been shown.

Circuit 14 is, for example, formed based on an operational amplifier 20, an inverting input terminal of which is connected, via a resistor R1, to terminal S. A low value capacitor C1 is placed between the inverting input of amplifier 20 and the ground. Cell R1C1 conditions the delay of the hysteresis of comparator 14 and is used for the filtering. The voltage reference is provided by a zener diode DZ, the anode of which is connected to the ground and the cathode of which is connected, via a resistor R2, to a non-inverting input terminal of amplifier 20. A decoupling capacitor C2 is mounted in parallel on diode DZ. The non-inverting input terminal of amplifier 20 is connected to its output via a resistor R3. The voltage amplitude of the hysteresis depends on the ratio between resistances R3 and R2. Amplifier 20 is supplied by voltage Ve. A resistor R4 is connected between the cathode of diode DZ and terminal 12, and a resistor R5 is placed between the output of the amplifier and terminal 12. The output of amplifier 20 is connected to the gates of two MOS transistors M5, M6, connected in series between terminal 12 and the ground. The midpoint of the series connection of transistors M5 (with a P channel) and M6 (with an N channel) is connected to the gate of transistor M2.

The function of resistor R5 is to enable the output of amplifier 20 to substantially reach potential Ve in the case where amplifier 20 is an open collector output stage amplifier.